REMARKS

The present response amends only the specification. Accordingly, claims 1, 2, 5-10, 12-16, and 18-20 are pending in the captioned case. Further examination and reconsideration of the presently claimed application are respectfully requested.

Objection to the Specification

An objection was lodged against the specification with regard to the term "typical" pertaining to Figs. 1a and 1b. In response to, the specification has been amended to remove the objectionable term. Accordingly, Applicants respectfully request removal of this objection.

Section 103 Rejection

Claims 1, 2, 5-10, 12-16, and 18-20 were rejected under 35 U.S.C. § 103(a) as being unpatentable over a combination of U.S. Patent No. 6,433,787 to Murphy (hereinafter "Murphy"), Applicant's admitted prior art (hereinafter "APA"), U.S. Patent No. 5,574,689 to Zaidi et al. (hereinafter "Zaidi"), and U.S. Patent No. 5,884,099 to Klingelhofer (hereinafter "Klingelhofer"). Applicants respectfully traverse this rejection on several grounds. Primarily, Applicants contend that the cited art fails to teach or suggest, when hypothetically combined, all features of the currently pending claims. As to each of the independent claims 1, 10, and 16, patentable distinctions will be set forth in more detail below.

As to claim 1, Murphy and APA do not teach or suggest: (i) N-bit read and N-bit write registers, (ii) a logic gate associated with each of the N storage locations for comparing the i^{th} bit in the write register with the i^{th} bit in the read register, or (iii) the status of the N storage locations being dependent on whether respective T tag bits are active. Present independent claim 1 recites various limitations, including the three patentably distinct limitation cited above. With reference to claim 1 and Figs. 1b and 2 of the present specification, the N-bit read and N-bit write registers are shown as items 22 and 24 in Fig. 2. Each register is N-bits long, corresponding to the number of rows in the FIFO 20. As data bits (d_i) are being written, the particular row being written to is identified with a bit via "aptr" of write register 22. Likewise, when bits are being read from the data lines or rows, the corresponding bit is indicated by a read pointer "bptr" of register 24.

Thus, the read and write registers are in communication with respective N storage locations (i.e., rows) and FIFO 20. For example, in the N-1 storage location or row, a comparison is made by logic gate 28 to the bit stored in the N-1 location of the read and write registers 22 and 24. Thus, logic gate 28 compares the i^{th} (in this case the N-1) bit in the write register with the i^{th} (i.e., N-1) bit in the read register, according to claim 1. This comparison yields a determination of which of the N storage locations have been written to and which have been read from. The status of the N storage locations output from the various logic gates, beginning with 0 and ending with N-1, at the outputs of logic gates 26 . . . 28 is further dependent on whether the T number of tag bits are active.

As shown in Fig. 2, the output from logic gates 26 . . . 28 are each fed into a series of AND gates. For example, the output from the N-1 logic gate 28, representative of the upper row of FIFO 20, is fed into a series of AND gates whose other input is the corresponding bits of T=0 through T=T-1. Thus, for each row of the FIFO, the EX OR gate will determine whether that row contains valid bits for the data word. Furthermore, the AND gates for each of the tag bits along that row will determine whether, for a valid row, a respective tag bit is active. Thus, the system of claim 1 determines the status of a storage device, where status is defined in the specification as to where the bits of that storage location were sourced or destined for a particular type of transaction. More importantly, the combination of "status" indicated by the tag bits and valid/invalid indicated by the read and write registers comparison, thereby determines for each of the N storage locations the source, destination, or type of transaction data exists within a valid or invalid storage location. For example, a user may only be interested in targeting a valid entry of a particular storage location that was destined for a particular peripheral device, or sourced from that peripheral device. *See, e.g.,* the present specification at page 2, line 5 - page 4, line 14.

As stated in the Office Action Mailed August 13, 2003 and, specifically, page 12 of that Office Action, Murphy in view of APA "does not teach an XOR [logic gate] associated with each N storage location comparing the i^{th} bit of the write register and the i^{th} bit of the read register." Thus, the previous Office Action concedes Murphy and APA do not render claim 1 obvious. Furthermore, since the Office Action admitted there is no logic gate associated with storage locations which compare read and write register bits, the Office Action also admits that there is no read and write registers cited in Murphy and/or APA. In fact, nowhere in Murphy is there any mention in connection with Fig. 3 that a separate read and write register exists for each of the FIFO 320 entries (Murphy -- Fig. 3; col. 8, lines 2-27).

Absent any suggestion whatsoever of read and write registers or a logic gate which compares register entries, Applicants respectfully assert that the combination of Murphy and APA cannot render obvious the teachings of claim 1. Moreover, Applicants respectfully traverse any suggestion that a validity flag 352 in Murphy is somehow an output of a XOR gate since, in fact, flag 352 is simply the flag set depending on whether the associated entry of data 350 is read or written (Murphy – col. 8, lines 19-27). Thus, the bits in flag 352 indicate the corresponding data is read data or written data, not whether an XOR function occurs that compares a bit in a write register with a bit in a read register to determine if the particular entry is valid or invalid, as recited in claim 1. The flag bits 352 in Murphy are simply not in any way the same or perform an identical function as an output of an XOR gate, and cannot be construed as such.

As to claim 10, the combination of Murphy, Zaidi, and Klingelhofer do not teach or suggest: (i) N-bit read and N-bit write registers to record which FIFO locations have been written to and which locations have been read, or (ii) the status of tag bits being detected in any FIFO location in which data has been written in lieu of being read. Similar to claim 1, claim 10 recites read and write registers to note which of the FIFO locations are valid (i.e., have been written to and not read). Moreover, claim 10 recites the similar status of tag bits as set forth in claim 1, where the tag bits are being detected in a particular FIFO location that is either valid or invalid. Thus, the status of the tag bits is given relevance based on whether the tag bits within a particular location 0 through N-1 correspond to valid or invalid entries in those locations. Thus, the tag bits are given significance on whether the device sources or receives valid or invalid data.

Thus, as claimed, it is simply not enough to know whether or not data is valid, but whether certain "tagged" data from a particular peripheral device or destined for a particular peripheral device contains valid data. If the data is not valid, then the present system and method can determine the status of that data before the data is even read. Combinatorial logic is used to quickly read valid and invalid statuses associated with data to determine possibly whether that data should even be used before fetching such data.

Like Murphy, Zaidi and Klingelhofer make no mention of a separate read and write register corresponding to each FIFO location, nor does the cited art teach or suggest logic which compares register contents or determines the status of tag bits based on those contents relative to any FIFO location. In fact, as stated in the Office Action Mailed August 13, 2003, agreement was reached as noted

on page 12 that the combination of Murphy, APA, Zaidi, and Klingelhofer does not teach two separate read and write registers, comparing of those registered contents, or determining a status of tag bits.

As to claim 16, Murphy, Zaidi, and Klingelhofer do not teach: (i) associating with each storage location a flag in a first register and a flag in a second register, (ii) comparing the state of the associated flag, (iii) detecting active tag bits with valid storage locations, or (iv) generating a logic signal for each of the tag bits such that the i^{th} logic signal is active if the i^{th} tag bit is active in any of the valid storage locations. Similar to claims 1 and 10, claim 16 recites separate registers and a comparison function for each of a corresponding set of N storage locations. Moreover, claim 16 recites the steps of detecting active tag bits with valid storage locations (i.e., validity being determined based on the comparison function). Still further, claim 16 recites the step of generating a logic signal of the tag bits depending on whether the i^{th} tag bit is active in any of the valid storage locations. Applicants agree with the characterizations made on page 13 of the Office Action Mailed August 13, 2003 which stated that the combination of cited art does not teach an indicator method for a storage device that associates a storage location flag in a pair of registers, nor does the cited art teach comparing the contents of the flags of corresponding storage locations to determine if the location has been written to and not read. Absent any suggestion of separate read and write registers or the comparison function of claim 16, Applicants respectfully traverse any suggestion that the combination of cited art could somehow render obvious claim 16 and claims dependent therefrom.

For at least the reasons stated above, Applicant believes that independent claims 1, 10, and 16 as well as claims dependent therefrom, are patentable over the cited art. Accordingly, Applicant respectfully requests removal of this rejection.

CONCLUSION

The present amendment and response is believed to be a complete response to the issues raised in the Office Action mailed July 28, 2004. In view of remarks traversing the objections and rejections, Applicants assert that pending claims 1, 2, 5-10, 12-16, and 18-20 are in condition for allowance. If the Examiner has any questions, comments or suggestions, the undersigned attorney earnestly requests a telephone conference.

No fees are required for filing this amendment. However, if a fee is required for the petition contained herein, the Commissioner is authorized to charge LSI Logic Corporation Deposit Account No. 12-2252/00-309.

Respectfully submitted,

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